ABSTRACT

A semiconductor apparatus comprises a processor having an instruction register inside thereof, a pseudorandom number generating device activated in response to a test operation and generating pseudorandom numbers, an input switchover device for switching over between data input in normal operation and input of the pseudorandom numbers from the pseudorandom number generating device in the test operation to thereby output the data or pseudorandom numbers to the instruction register. The pseudorandom numbers generated in the pseudorandom number generating device are inputted to the instruction register via the input switchover device so that the random instructions are implemented and a random test is implemented with an activation rate equivalent to the same in the normal operation.